Claims

[c1] What is claimed is:

1. A control method of a non-volatile memory, the non-volatile memory comprising a plurality of memory cells, each memory cell comprising:

a substrate;

a storage unit positioned on the substrate for storing data, the storage unit comprising:

a floating gate for storing charges; and

a control gate for receiving an operational voltage to induce a conductive channel on the surface of the substrate, the conducting channel being related to a total number of charges stored on the floating gate; and

a control unit positioned on the substrate, a parasitic capacitor between the control unit and the storage unit being affected by establishment of the conducting channel;

the control method comprising:

applying a first predetermined voltage to the control unit; and

measuring a voltage shift of the first predetermined voltage to determine data stored in the storage unit after the first predetermined voltage is passed through the parasitic capacitor.

[c2] 2. The control method of claim 1 wherein the storage unit further comprises:

a first oxide layer positioned between the substrate and the floating gate for isolating the substrate from the floating gate; and

a second oxide layer positioned between the control gate and the floating gate for isolating the control gate from the floating gate.

[c3] 3. The control method of claim 2 wherein the floating gate is a poly-silicon layer that is a conductor.

[c4] 4. The control method of claim 2 wherein the floating gate is a nitride layer that is a nonconductor.

[c5] 5. The control method of claim 1 wherein the control unit is a metal-oxide-semiconductor (MOS) transistor comprising:

a first electrode for receiving a control voltage to control conductivity of the

control unit;

a second electrode for receiving the first predetermined voltage, a second predetermined voltage, and a third predetermined voltage to adjust charges stored in the parasitic capacitor so that corresponding data represented by amounts of the charges are stored; and

a third electrode electrically connected to the parasitic capacitor.

[c6] 6. The control method of claim 5 wherein the first predetermined voltage is less than the second predetermined voltage but greater than the third predetermined voltage.

[c7] 7. The control method of claim 6 wherein the second predetermined voltage stands for a binary value "1", and the third predetermined voltage stands for a binary value "0".

[c8] 8. The control method of claim 7 further comprising adjusting a voltage level of the third electrode to approach the second predetermined voltage or the third predetermined voltage according to amounts of charges stored on the floating gate.

[c9] 9. The control method of claim 8 further comprising:

passing an input voltage to the control gate of each memory cell for inducing the conductive channel on the surface of the substrate of each memory cell so as to force the parasitic capacitor of each memory cell to approach a predetermined capacitance.

[c10] 10. The control method of claim 1 further comprising adjusting amounts of charges stored on the floating gate to record the corresponding data according to the voltage shift.

[c11] 11. The control method of claim 10 further comprising:

adjusting amounts of the charges stored on the floating gate to be greater than a predetermined storage number if the voltage shift is positive; and

adjusting amounts of the charges stored on the floating gate to be less than the predetermined storage number if the voltage shift is negative.